UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,635	07/29/2003	Jeffrey Jay Rooney	MTIPAT.002C1C1	9052

20995 7590 03/10/2006

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
PARK, ILWOO	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,635	ROONEY, JEFFREY JAY	
	Examiner	Art Unit	
	Ilwoo Park	2182	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-7,9-12,14-17,19-29,31-35,37 and 39-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-7,9-12,14-17,19-29,31-35,37 and 39-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 8, 13, 18, 30, 36, and 38 are canceled, claims 2-5, 7, 10, 11, 16, 17, 20, 22, 23, 31-35, and 37 are amended, and claim 43 is added in response to the last office action. The following rejections now apply. Bennett, Coke, Rabe et al, Rice, and Lange were cited in the last office action. Claims 2-7, 9-12, 14-17, 19-29, 31-35, 37, and 39-43 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 2-7, 9-12, 14-17, 19-21, 23-29, 31, 33-35, 37, and 39-42 are rejected under 35 U.S.C. 102(b) as being anticipated by Solari, US patent No. 5,333,276.

As to claim 2, Solari teaches a method for providing data transfers between a processor [processor 122 in fig. 1b] and a component [e.g., ref. Nos. 132-135, 142-144 in fig. 1b], the method comprising:

buffering [col. 2, lines 57-59] a first address with a first address buffer and a second address with a second address buffer, the first and second address buffers

being in communication with a processor and a component, wherein the processor operates at a different speed [col. 5, lines 5-12] than the component;

buffering [col. 2, lines 57-59] a first data value with a first bi-directional data buffer and buffering a second data value with a second bi-directional buffer, the first and second bi-directional buffers [col. 2, lines 55-57] being in communication with the processor and the component;

controlling [col. 7, lines 35-52] the first address buffer and the first bi-directional data buffer as a matched pair such that the first address held in the first address buffer corresponds to the first data value held in the first bi-directional buffer; and

controlling [col. 8, lines 58-61; col. 11, lines 11-28; col. 13, lines 48-61] the order of bi-directional data flow through the first and second first bi-directional buffers such that data flows between the processor and the component, wherein the controlling the order of the data flow is based on a priority status of the first and second data values.

4. As to claim 3, Solari teaches the first and second bi-directional buffers are in communication with the processor via a bus [fig. 1a].

5. As to claim 4, Solari teaches the first and second bi-directional buffers are in communication with a bus master controller and a bus slave controller [address FIFO input/output controls in fig. 2a].

6. As to claim 5, Solari teaches the first address buffer further comprises status bits [figs. 3a-c].

7. As to claim 6, Solari teaches the status bits relate to the type of request being made by the processor [figs. 3a-3c].

8. As to claim 7, Solari teaches said controlling said first address buffer and the first bi-directional data buffer as matched pair is performed with pointers [col. 9, lines 15-23].

9. As to claim 9, Solari teaches said act of controlling bi-directional data flow is performed with at least one input data arbiter [col. 9, lines 12-23].

10. As to claim 10, Solari teaches a method for controlling data transfers between a processor [processor 122 in fig. 1b] and a component [e.g., ref. Nos. 132-135, 142-144 in fig. 1b], the method comprising:

buffering [col. 2, lines 57-59] with a plurality of address buffers address requests from a processor to a component, wherein the processor operates at a different speed [col. 5, lines 5-12] than the component;

bi-directionally buffering [col. 2, lines 55-59] with a plurality of bi-directional data buffers data transfers between the processor and the component, wherein said data transfers are performed out of order [col. 8, lines 58-61; col. 11, lines 11-28; col. 13, lines 48-61] based on a priority status of each of the data transfers; and

controlling [col. 7, lines 35-56] said buffering address requests and said bi-directionally buffering such that each of the buffered data transfers relates to an address held in one of the plurality of address buffers.

11. As to claim 11, Solari teaches indicating which of the plurality of bi-directional data buffers is available to accept new data [col. 10, lines 47-53].

12. As to claim 12, Solari teaches said act of indicating is performed with reference pointers [col. 9, lines 12-23].

13. As to claim 14, Solari teaches said act of buffering address requests includes the use of an input arbiter and an output arbiter [col. 9, lines 12-23].

14. As to claim 15, Solari teaches said act of bi-directional buffering is performed with an input arbiter and an output arbiter [col. 9, lines 12-23].

15. As to claim 16, Solari teaches the plurality of address buffers comprises at least three address buffers and wherein the plurality of bi-directional data buffers comprises at least three bi-directional data buffers [figs. 2a-2b].

16. As to claim 17, Solari teaches a method for providing data transfers between a processor [processor 122 in fig. 1b] and a component [e.g., ref. Nos. 132-135, 142-144 in fig. 1b], the method comprising:

buffering [col. 2, lines 57-59; fig. 2a] a first address buffer with a first address;

buffering [col. 2, lines 57-59; fig. 2a] a second address buffer with a second address;

buffering [col. 2, lines 57-59; fig. 2b] a first data buffer with a first data value;

buffering [col. 2, lines 57-59; fig. 2b] a second data buffer with a second data value;

controlling [col. 7, lines 35-52] the first address buffer and the first data buffer as a first matched pair such that the first address corresponds to the first data value;

controlling [col. 7, lines 35-52] the second address buffer and the second data buffer as a second matched pair such that the second address corresponds to the second data value; and

controlling [col. 8, lines 58-61; col. 11, lines 11-28; col. 13, lines 48-61] bi-directional data flow through the first data buffer and the second data buffer such that data flows between a processor and a component, wherein said controlling is based at least in part on a priority value associated with the data.

17. As to claim 19, Solari teaches the first and second address buffers and the first and second data buffers are in communication with the processor via a bus [fig. 1a].

18. As to claim 20, Solari teaches said act of controlling the first address buffer and the first data buffer as a first matched pair is performed with pointers [col. 9, lines 12-23].

19. As to claim 21, Solari teaches said act of controlling bi-directional data flow is performed with at least one input data arbiter [col. 9, lines 12-23].

20. As to claim 23, Solari teaches a method of transferring addresses and data through a bi-directional buffer [col. 2, lines 55-57], the method comprising:

storing [col. 2, lines 57-59] a first address in a first buffer in communication with a first component and a second component [e.g., ref. Nos. 132-135, 142-144 in fig. 1b], the first buffer including status bits [figs. 3a-3c];

storing [col. 7, lines 35-52] first data in a second buffer matched with said first buffer so that the first address storied in the first buffer is related to the first data stored in the second buffer;

storing [col. 2, lines 57-59] a second address in a third buffer in communication with a first component and a second component [e.g., ref. Nos. 132-135, 142-144 in fig. 1b];

storing [col. 7, lines 35-52] second data in a fourth buffer matched with said third buffer so that the second address storied in the third buffer is related to the second data stored in the fourth buffer;

determining [col. 8, lines 58-61; col. 11, lines 11-28; col. 13, lines 48-61] a first priority value of the first data and determining a second priority data value on the second data; and

controlling [col. 8, lines 58-61; col. 11, lines 11-28; col. 13, lines 48-61] the order of data flow of the first data and the second data based at least in part on said

21. As to claim 24, Solari teaches the status bits comprise transfer type bits indicative of the status of an address transfer from the first component to the first buffer [figs. 3a-3c].

22. As to claim 25, Solari teaches the status bits comprise transfer type bits indicative of the status of a data transfer from the first component to the first buffer [figs. 3a-3c].

23. As to claim 26, Solari teaches the first component comprises a memory [fig. 1b].

24. As to claim 27, Solari teaches the first component comprises a processor [fig. 1b].

25. As to claim 28, Solari teaches the first buffer is in communication with the processor via a bus [fig. 1b].

26. As to claim 29, Solari teaches the first buffer is in communication with the processor via a bus master controller and a bus slave controller [address FIFO input/output controls in fig. 2a].

27. As to claim 31, Solari teaches a method of transferring data between a between a processor [processor 122 in fig. 1b] and a component [e.g., ref. Nos. 132-135, 142-144 in fig. 1b] utilizing a plurality of address buffers and a plurality of data buffers [figs. 2a-2b], the method comprising:

receiving [col. 13, lines 48-68] a data request including an associated address from a processor;

determining [col. 10, lines 47-53] whether at least one of a plurality of address buffers and an associated [col. 7, lines 35-52] bi-directional data buffer are available;

storing [col. 2, lines 57-59] the associated address in the at least one address buffer;

receiving [fig. 8a] data identified by the associated address from the component with the bi-directional data buffer

ordering [fig. 8a; col. 13, lines 48-68], based on a priority of the data request, the transmission of the data from the bi-directional data buffer to a processor.

28. As to claim 33, Solari teaches the at least one address buffer and the bi-directional data buffer are in communication with the processor via the bus [fig. 1b].

29. As to claim 34, Solari teaches the at least one address buffer and the bi-directional data buffer are in communication with the bus via a bus master controller and a bus slave controller [address FIFO input/output controls in fig. 2a].

30. As to claim 35, Solari teaches the bi-directional data buffer and the at least one address buffer are associated with each other through the use of pointers [col. 9, lines 12-23].

31. As to claim 37, Solari teaches an apparatus for controlling data transfers between a processor [processor 122 in fig. 1b] and a component [e.g., ref. Nos. 132-135, 142-144 in fig. 1b], the apparatus comprising:

means for buffering [col. 2, lines 55-59] address requests from a processor to a component;

means for bi-directionally buffering [col. 2, lines 55-59] data transfers between the processor and the component; and

means for controlling [col. 7, lines 35-52] the means for buffering and the means for bi-directionally buffering so that each of the buffered data transfers relates to an address held in the means for buffering, wherein the means for controlling further coordinates [col. 8, lines 58-61; col. 11, lines 11-28; col. 13, lines 48-61] said data transfers based at least on a priority status of each buffered data transfer.

32. As to claim 39, Solari teaches means for buffering includes a plurality of address buffers [fig. 2a].

33. As to claim 40, Solari teaches means for bi-directionally buffering includes a plurality of data buffers [fig. 2b].

34. As to claim 41, Solari teaches means for buffering includes an input arbiter and an output arbiter [col. 9, lines 12-23].

35. As to claim 42, Solari teaches means for bi-directionally buffering includes an input arbiter and an output arbiter [col. 9, lines 12-23].

Claim Rejections - 35 USC § 103

36. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

37. Claims 22, 32, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Solari, US patent No. 5,333,276 in view of Rabe et al., US patent No. 5,664,122.

As to claims 22, 32, and 43, Solari teaches controlling the first separate address buffer and the first separate data buffer as a first matched pair. However, Solari does not explicitly disclose the buffer control allowing data to be read from the first data buffer while an address is written to the first address buffer. Rabe et al teach a method for providing data transfers between a processor and a component controlling a first separate address buffer and a first separate data buffer and the buffer control allowing data to be read from a first data buffer while [col. 8, lines 56-64; col. 9, lines 43-51] an address is written to a first address buffer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the buffer control allowing data to be read from a first data buffer while an address is written to a first address buffer in order to expedite the immediate priority data transfer control between a processor and a component of Solari.

Conclusion

38. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ilwoo Park whose telephone number is (571) 272-4155. The examiner can normally be reached on Monday through Friday from 9:00 AM to 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ILWOO PARK
PRIMARY EXAMINER

Ilwoo Park
March 2, 2006